WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a semiconductor memory circuit which includes a memory cell array including a plurality of memory cells in a matrix form each constituted of a cell transistor and a ferroelectric capacitor connected in parallel between source and drain terminals of the cell transistor, a plurality of word lines connected to gates of the cell transistors, a plurality of pairs of bit lines, a plurality of block selection transistors each connected between one end of the memory cells connected in series in a corresponding row and a corresponding bit line, a plurality of plate lines each connected to the other end of the memory cells connected in series in the corresponding row, and a plurality of sense amplifier circuits each connected to a corresponding pair of bit lines; and

a control circuit which controls the semiconductor memory circuit in an operation time to raise gate potentials of the block selection transistors to be selected from a first potential to a second potential to read cell data from the memory cells of the selected block selection transistors onto the bit lines, thereafter set the bit lines to a high level to write "1" data into the memory cells regardless of a logic level of data to be written, thereafter set the gate potentials of the selected block selection transistors to a third potential lower than the second potential and higher than the first potential, set the bit line to a low level with "0" data to be written to write "0" data into the memory cells, and thereafter to lower the gate potentials of the selected block selection transistors to the first potential.

2. The semiconductor memory device according to claim 1, further comprising:

a plurality of separating transistors each disposed on each of a corresponding pair of bit lines between the memory cell array and the sense amplifier circuit; and

a plurality of precharge circuits each for precharging a corresponding pair of bit lines on a side of the memory cell array at a high level, wherein the separating transistors are turned off after reading the cell data onto the bit lines from the memory cells, and are turned on after setting the gate potentials of the selected block selection transistors to the third potential lower than the second potential and higher than the first potential.

3. The semiconductor memory device according to claim 1, wherein in an operation time potentials of the word lines of the memory cells to be selected are lowered to Vss, and potentials of the word lines of the memory cells between the selected memory cells and the block selection transistors are set to the second potential in writing of "1" data, and set to the third potential in writing of "0" data.

4. The semiconductor memory device according to claim 1, wherein the plate lines are set to the low level in a standby time and are raised from the low level to the high level in an operation time.